3T1D MEMORY CELLS USING GATED DIODES AND METHODS OF USE THEREOF

Abstract of the Disclosure

A memory cell comprises: (1) a write switch, the first terminal of the write switch coupled to an at least one bitline, the control terminal of the write switch coupled to the first control line; (2) a two terminal semiconductor, the first terminal of the two terminal semiconductor device coupled to the second terminal of the write switch, and the second terminal of the two terminal semiconductor device coupled to an at least one second control line, wherein the two terminal semiconductor device has a capacitance when a voltage on the first terminal relative to the second terminal is above a threshold voltage and has a lower capacitance when the voltage on the first terminal relative to the second terminal is less than the threshold voltage; (3) a read select switch, the control terminal of the read select switch coupled to an at least one second control line, the first terminal of the read select switch coupled to the at least one bitline; and (4) a read switch, the control terminal of the read switch coupled to the first terminal of the gated diode and coupled to the second terminal of the write switch, the first terminal of the read switch coupled to the second terminal of the read select gate, and the second terminal of the read switch coupled to ground.